REMARKS/ARGUMENTS

In the Office Action notified on September 12, 2008, claims 1 and 3-11 are rejected. In response, claims 1 and 5-11 have been amended, claim 4 has been canceled and new claims 12 and 13 have been added. Applicants hereby request reconsideration of the application in view of the claim amendments, the new claims, and the below-provided remarks.

Claim Rejections under 35 U.S.C. 103

Claims 1 and 3-11 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Moller et al. (U.S. Pat. Pub. No. 2003/0014653, hereinafter "Moller") in view of McClain et al. (U.S. Pat. No. 6,731,536, hereinafter "McClain"). In response, claims 1 and 5-11 have been amended, claim 4 has been canceled and new claims 12 and 13 have been added. Applicants respectfully submit that the pending claims are patentable over the cited references for the reasons provided below.

Independent Claim 1

Claim 1 has been amended to include all of the limitations of claim 4. Thus, claim 4 has been canceled. Additionally, claim 1 has been amended to correct informalities. Support for the amendments to claim 1 is found in Applicants' specification at, for example, original claims 1 and 4, and page 6, lines 10-19.

As amended, claim 1 recites in part that "*said protected data includes data to activate/deactivate an optional feature of the chip*" (emphasis added), which is not taught by Moller. Thus, Applicants respectfully assert that amended claim 1 is not obvious over Moller in view of McClain.

Moller teaches that a memory device (100) includes a protection control register (PCR), which contains enabling or disabling information for data interfaces connected to the memory device (100). (See Fig. 1 and paragraphs [0012], [0022] and [0024]). The Office Action states that the data interface enabling or disabling information in the protection control register (PCR) is equivalent to "protected data" (emphasis added), as

recited in claim 1. (See page 4, the rejection to claim 4 of the Office Action). Applicants respectfully disagree.

Applicants respectfully assert the data interface enabling or disabling information in the protection control register (PCR) is more equivalent to "protection data" (emphasis added), as recited in claim 1. In particular, claim 1 recites in part "*said protection data being intended to define a protection level for authorizing/denying access to said protected data by said microprocessor while a program is executed, wherein said protection data is only modifiable so as to increase said protection level*" (emphasis added). Moller teaches that the contents of the protection control register (PCR) in on-state can be changed only in one direction, which is from enabling a data interface to disabling the data interface. (See paragraph [0028]). However, Moller does not teach that data in any other memory block of the memory device (100) define a protection level for authorizing/denying access to protected data and is only modifiable so as to increase the protection level. That is, the data interface enabling or disabling information in the protection control register (PCR) is equivalent to the "protection data" (emphasis added), as recited in claim 1. Because the contents in the protection control register (PCR) are equivalent to the "protection data" (emphasis added), as recited in claim 1, the contents in the protection control register (PCR) are not the "protected data" (emphasis added), as recited in claim 1. Thus, Moller fails to teach that "*said protected data include data to activate/deactivate an optional feature of the chip*" (emphasis added), as recited in claim 1.

Because Moller fails to teach the above-identified limitation of claim 1, Applicants respectfully assert that Moller in view of McClain fails to teach all of the limitations of claim 1. Thus, Applicants respectfully assert that claim is not obvious over Moller in view of McClain.

Dependent Claims 3 and 5-8

Claims 5-8 have been amended to correct informalities. Additionally, claims 5 and 6 have been amend to reflect claim dependency changes. Support for the amendments to claims 5-8 is found in Applicants' specification at, for example, original claims 1 and 4-8.

Claims 3 and 5-8 depend from and incorporate all of the limitations of independent claim 1. Thus, Applicants respectfully assert that claims 3 and 5-8 are allowable at least based on an allowable claim 1. Additionally, claims 5 and 6 may be allowable for further reasons, as described below.

Claim 5 recites in part that "*said optional feature is a connection to an external device for downloading a program and/or data from said external device.*" Claim 6 recites in part that "*said protected data includes data to activate/deactivate an external boot program for said microprocessor, said external boot program including instructions for downloading a new boot program for said microprocessor from an external memory.*" The above-identified limitations of claims 5 and 6 further define the limitation "*said protected data includes data to activate/deactivate an optional feature of the chip*" of claim 1.

As described above, the data interface enabling or disabling information in the protection control register (PCR) is not "protected data" (emphasis added), as recited in claim 1. Thus, Moller fails to teach that "*said protected data includes data to activate/deactivate an optional feature of the chip*" (emphasis added), as recited in claim 1. Because the above-identified limitations of claims 5 and 6 further define the limitation "*said protected data includes data to activate/deactivate an optional feature of the chip*" of claim 1, Applicants respectfully assert that Moller also fails to teach the above-identified limitations of claims 5 and 6.

Independent Claim 9

Claim 9 has been amended in a similar fashion as claim 1. Support for the amendments to claim 9 is found in Applicants' specification at, for example, original claims 1, 4, and 9, and page 6, lines 10-19. As amended, claim 9 includes similar limitations to claim 1. Because of the similarities between claim 9 and claim 1, Applicants respectfully assert that the remarks provided above with regard to claim 1 apply also to claim 9. Accordingly, Applicants respectfully assert that claim 9 is not obvious over Moller in view of McClain.

Dependent Claim 10

Claim 10 has been amended to correct informalities. Claim 10 depends from and incorporates all of the limitations of independent claim 9. Thus, Applicants respectfully assert that claim 10 is allowable at least based on an allowable claim 9.

Independent Claim 11

Claim 11 has been amended in a similar fashion as claim 1. Support for the amendments to claim 11 is found in Applicants' specification at, for example, original claims 1, 4, and 11, and page 6, lines 10-19. As amended, claim 11 includes similar limitations to claim 1. Because of the similarities between claim 11 and claim 1, Applicants respectfully assert that the remarks provided above with regard to claim 1 apply also to claim 11. Accordingly, Applicants respectfully assert that claim 11 is not obvious over Moller in view of McClain.

New Claims 12 and 13

Claims 12 and 13 have been added. Support for claim 12 is found in Applicants' specification at, for example, original claim 1, page 12, lines 21-23 and page 13, lines 14-17. Support for claim 13 is found in Applicants' specification at, for example, original claim 1 and page 12, lines 20 and 21. Claims 12 and 13 depend from and incorporate all of the limitations of independent claims 1. Thus, Applicants respectfully assert that claims 12 and 13 are allowable at least based on an allowable claims 1. Additionally, claims 12 and 13 may be allowable for further reasons, as described below.

Claim 12 recites in part "*a random logic coupled between said integrated non-volatile programmable memory and a connection bus of said microprocessor.*" Applicants respectfully assert that Moller fails to teach the above-identified limitation of claim 12. In particular, Moller teaches that a processor core (11) connects a static random-access memory (SRAM) (15) and a flash memory (1) via a data bus (12) or an address bus (13). (See Fig. 5 and paragraphs [0037] and [0038]). That is, Moller teaches that the SRAM (15) and the flash memory (1) are directly connected to the data bus (12) and the address bus (13) of the processor core (11). Because Moller teaches that the SRAM (15) and the flash memory (1) are directly connected to the data bus (12) and the

address bus (13) of the processor core (11), Moller fails to teach that there is a random logic between any of the SRAM (15) and the flash memory (1) and any of the data bus (12) and the address bus (13) of the processor core (11). Thus, Applicants respectfully assert that Moller fails to teach the above-identified limitation of claim 12.

Claim 13 recites in part that "*said microprocessor is a processor having a MIPS instruction set.*" Applicants respectfully assert that Moller in view of McClain fails to teach the above-identified limitation of claim 13. In particular, Moller teaches that a microprocessor includes a memory device to be protected. (See paragraphs [0006], [0022] and [0037]). McClain teaches that as virtually every sector of technology moves toward microprocessor controlled functionality, the need for effective protection of code controlling the microprocessor becomes increasingly important. (See column 1, lines 11-14). However, Moller and McClain fail to teach that any of the processors is "a *processor having a MIPS instruction set,*" as recited in claim 13. Thus, Applicants respectfully assert that Moller in view of McClain fails to teach the above-identified limitation of claim 13.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

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